

## REMARKS

This is intended as a full and complete response to the Final Office Action dated December 26, 2007, having a shortened statutory period for response set to expire on March 26, 2007. Claims 1-5, 8-12, 15-17, 19-25 are pending in the application. Claims 1-5, 8-12, 15-17, 19-21 are rejected under 35 U.S.C. § 102(e) as anticipated by Hayes (U.S. 2003/0158906). Claims 22-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes.

Claims 1, 9, and 16 each recite limitations of a user buffer in a first portion of memory that is allocated to an application program and a legacy buffer in a second portion of the memory that is allocated to a software driver configured to communicate between an offload unit and a TCP stack. Hayes fails to teach or suggest these limitations.

In Figure 7, Hayes shows memory 108, but does not teach or suggest that frame data is stored in this memory. In particular, Hayes fails to teach or suggest that portions of the memory are allocated to both a software driver and an application program.

The Examiner relies on a single sentence in paragraph [0003] of Hayes for the teachings of the claimed user buffer and legacy buffer, “[m]ore particularly, one preferred embodiment of the invention enables the offloading auxiliary processor to deposit incoming user data directly into the user’s memory space, bypassing the placing of a copy of the data into the operating system’s memory...”. In focusing on this sentence, the Examiner equates the incoming user data with a frame, the user’s memory space with the first portion of memory that is allocated to the application program, and the operating system’s memory with the second portion of the memory that is allocated to the software driver, which is configured to communicate between an offload unit and a TCP stack. Neither the user’s memory space nor the operating system’s memory is illustrated in any of the Figures of Hayes or described in the specification. Therefore, the general statement does not rise to the level of a teaching required to anticipate or render obvious the pending claims.

Nowhere does Hayes specify where the user’s memory space is located or to which function the user’s memory space is allocated. As described in paragraph [0003]

of Hayes, one purpose of the auxiliary processor is to reduce the memory bandwidth consumed compared with having the CPU perform protocol processing tasks. It follows from such a purpose that the user's memory space would be located in NIC 26 of Figure 7 in order to reduce the memory bandwidth to memory 108 when NIC 26 offloads protocol processing tasks from CPU 28. Presumably, the operating system's memory is located within memory 108 and allocated to the operating system. With such an architecture, depositing user data in user memory in NIC 26 would reduce the memory bandwidth of memory 108, compared with depositing user data in memory 108. Such an architecture is completely in-line with the basic teachings of the Hayes reference, but this architecture clearly does not satisfy the limitations of the pending claims. Again, the one sentence cited by the Examiner is simply too broad to conclude that it teaches or suggests the architecture covered by the pending claims.

Additionally, claims 1, 9, and 16 of the present application recite the specific limitation that the second portion of the memory is allocated to a software driver that is configured to communicate between an offload unit and a TCP stack. The software driver provides this communication to supplement the functions performed by the operating system. The software driver is separate from the memory allocated to the operating system and is allocated memory that is separate from the operating system. Therefore, the second portion of memory that stores the legacy buffers is not the same as the "operating system memory" of Hayes.

In addition to failing to teach the claimed user buffers and legacy buffers, Hayes also fails to teach that frames are uploaded to those buffers. As noted by the Examiner, Figure 12 of Hayes illustrates the steps performed during the offloading process. According to Figure 12, portions of packets are sent to various drivers or to a default destination. Two of the drivers are located in offload host computer 12, and the remaining driver is located in NIC 26c (as shown in Figure 10). The default destination is not described at all in the Hayes reference. Hayes fails to describe any memory being associated with the various drivers or default destination. Since Hayes fails to discuss the memories associated with the drivers or the default destination, Figure 12 cannot show that portions of the packets are uploaded to buffers in memory, as recited

in the pending claims. Thus, Hayes does not teach the limitations recited in claims 1, 9, and 16 of the present application.

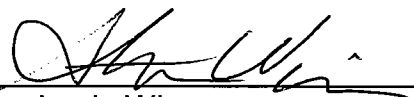
Upon a thorough reading of Hayes, Applicant fails to find any teaching related to issuing an interrupt to the CPU, as stated by the Examiner regarding claim 21 of the present application. In fact, Hayes has no disclosure relating to issuing an interrupt to the CPU. Therefore, Hayes cannot teach or suggest the limitations recited in claim 21. Claims 22-25 recite the limitations of user buffers and legacy buffer that are stored in physically contiguous and non-contiguous memory locations. Again, Hayes is silent regarding the physical locations of buffers, and therefore Hayes fails to teach or suggest these limitations as well.

For the foregoing reasons, Applicants submit that Hayes fails to teach or suggest the limitations recited in independent claims 1, 9, and 16. Therefore, claims 1, 9, 16 and their respective dependent claims are patentable over Hayes.

### CONCLUSION

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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